REMARKS

Claims 9-28 are pending in the present application. Claims 25-27 were previously amended.

Applicants are pleased to note that the Examiner has indicated that claims 14-15, 20-21 and 27 would be allowable if rewritten to include all of the limitations of the claims from which they depend.

Applicants respectfully request reconsideration of the application in view of the remarks appearing below.

Rejection Under 35 U.S.C. § 103

The Office Action presents a rejection of claims 9-13, 16-19, 22-26 and 28 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,526,559 to Schiefele et al. ("the Schiefele patent"). Applicants respectfully disagree.

The Schiefele patent provides a field programmable gate array (FPGA) with dynamic reconfiguration in time multiplexing fashion. Duplicate copies are configured in a time multiplexing manner which are functionally identical to a primary circuit specified for a predetermined FPGA's application. The primary and duplicate circuits are interrogated by a voting circuit which determines the existence of a faulted circuit in order to eliminate the faulted circuit from the operation of the FPGA.

Applicants' claimed invention is a hardware-implemented fault protection method and system used to design a circuit so that it is able to continue working properly in the presence of a hardware fault by using redundancy for select logic functions. Plainly stated, Applicants' claimed invention allows an integrated circuit designer to designate, during the design phase, particular logic functions to be fault tolerant using a fault tolerant operator. Those designated logic functions are then redundantly built on the integrated circuit. A voter is also built on the circuit to ensure that the outputs of all redundant logic functions are the same. If one of the logic functions fails (i.e., produces a different output than the others), that particular logic function is disabled, thereby allowing the integrated circuit to continue to operate properly.

With respect to independent claims 9, 16 and 23, the Office Action asserts that the Schiefele patent teaches a method and system for creating circuit redundancy in programmable logic, comprising the steps of (a) creating an integrated circuit design description using a hardware design language, (b) adding a fault tolerant operator to the particular logic functions in

said integrated circuit design description, and (c) building redundant copies for the particular logic functions having a fault tolerant operator.

Claims 9, 16, and 23 each require "adding a fault tolerant operator to the particular logic functions in said integrated circuit design description," or a slight variation of such language, to designate the particular logic functions as fault tolerant. Designation of fault tolerant functions allows a designer to specify which particular logic functions need redundant copies. During the design stage, the designer has the flexibility to trade off between a chip size and fault tolerance levels according to specific application requirements.

In rejecting these claims, the Office Action refers Applicants to col. 1, ll. 14-15 and col. 13, ll. 49-67, of the Schiefele patent. However, the Schiefele patent, at these or any location, is completely silent as to adding a fault tolerant operator to particular logic functions. For example, at col. 1, ll. 14-15, the Schiefele patent discloses dynamically reconfigurable FPGAs where redundant circuits are created in a time multiplexing manner. Moreover, at col. 13, ll. 49-67, the Schiefele patent provides steps for submitting the HDL to the compiler; separating the place and route output from the previous step for the primary, 1st duplicate, and 2nd duplicate, etc.; defining the HDL for the overlap region of the circuit; operating the compiler is operated in incremental mode to produce the place and route for the entire primary circuit; and forming the final configuration file for the first virtual equivalent.

Additionally, claim 9 requires "building redundant copies for the particular logic functions having a fault tolerant operator." Claims 16 and 23 each require including a fault redundant scheme in the integrated circuit design description for each logic function having a fault tolerant operator. The redundant copies of the particular logic function with a fault tolerant operator are created at the same time in Applicants' claimed invention. In contrast, the Schiefele patent utilizes a time multiplexing technique that requires the FPGA to be dynamically reconfigured multiple times to implement each redundant copy of the circuit prior to voting. (Col. 6, ll. 20-26).

Accordingly, the Schiefele patent does not disclose, teach, suggest or even hint at adding a fault tolerant operator to particular logic functions and building redundant copies for the particular logic function having a fault tolerant operator.

The differences between the independent claims 9, 16, and 23 and the subject matter of the Schiefele patent also apply to the dependent claims 10-13, 17-19, 22, 24-26, and 28. As

such, Applicants respectfully submit all claims in the present application are believed to be novel over the Schiefele patent.

In view of the preceding comments, it is clear that Applicants' claimed invention is novel over the Schiefele patent. Further, there is not even the slightest suggestion in the Schiefele patent or elsewhere that the invention described therein could be expanded to cover Applicants' claimed invention.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection.

CONCLUSION

In view of the foregoing, Applicants submit that claims 9-28 are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully solicited. If any issues remain or if the Examiner continues to believe that the Applicants' invention is anticipated by the Schiefele patent, Applicants respectfully request that the Examiner contact the undersigned attorney at the number listed below to conduct an interview with respect to the outstanding issues.

Respectfully submitted,

INTERNATIONAL BUSINESS MACHINES CORPORATION

By: Norman S. Yi

Norman S. Yi
Registration No.: 58,268
DOWNS RACHLIN MARTIN PLLC
Tel: (802) 863-2375
Attorneys for Applicants

BTV.497548.1